IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
Garg *et al.*	Art Unit: 2783
Appl. No.: 08/937,361	Examiner: L. Donaghue
Filed: September 25, 1997	Batch No.: E84
For: **RISC Microprocessor Architecture Implementing Multiple Typed Register Sets**	Atty. Docket: SP018.C3

Amendment under 37 C.F.R. § 1.312(a)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herein is an Amendment under 37 C.F.R. § 1.312(a). As payment of the issue fee has not yet been made or is filed herewith, Applicants respectfully submits that filing under paragraph (a) of 37 C.F.R. § 1.312 is proper. (M.P.E.P. § 714.16.)

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Deposit Account No. 19-0036.

Please enter the following amendments:

In the Claims:

8 (AMEND)

38. The apparatus of claim 36, further comprising processing means for executing instructions including Boolean execution unit to execute Boolean combinational instructions each operating on one or more Boolean operands to generate a Boolean result, each Boolean combinational instruction including one or more Boolean fields specifying a location of each operand and result, an integer execution unit[.] to execute integer instructions each operating on one or more integer operands to generate an integer result, each integer instruction including one or more integer fields specifying a location of each operand and result, and a floating point